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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,760	06/15/2001	Shuo-Yen Robert Li	Li7	1794

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EXAMINER	
LEE, ANDREW CHUNG CHEUNG	
ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,760	LI ET AL.	
	Examiner	Art Unit	
	Andrew C. Lee	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/05/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 2, 4, 5, 6, 7, 9, 10, 12, 13, 15, 16, 17, 18, 20, 21, 22, 23, 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limits for the parameters M, N, N_1, N_2 and B are not defined and specified clearly.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5, 9, 12, 13, 16, 20, 21, 24, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (U.S. 5801641 B1) in view of Eng et al. (U.S.4955017).

Regarding claims 1, 12, 21, 24, Yang et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (column 3, lines 52 – 57; column 6, lines 54 – 61), the switch comprising an input module, having M inputs and B outputs, B>M, for switching the M

input packets to M of the B outputs to produce M switched packets during each of the frame times (column 6, lines 54 – 61), a packet buffer including B registers, coupled to the input module, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets (column 11, lines 32 – 37), and an output module, having B inputs and N outputs coupled to the packet buffer (Fig. 2B, element 22, output stage; column 11, lines 32 – 37), Yang et al. do not disclose expressly for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses contained within each of the stored packets. Eng et al. disclose for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses contained within each of the stored packets (column 2, lines 60 – 65; column 6, lines 66 – 68, column 7, lines 1 – 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yang et al. to include for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses contained within each of the stored packets such as that taught by Eng et al. in order to provide in cases where no excess packet dropping is allowed, additional buffers can be provided to temporarily store the excess packets for retransmission (as suggested by Eng et al. see column 2, lines 5 – 8).

Regarding claims 2, 13, Yang et al. discloses the limitation of the packet switch as recited in claim 1 wherein the input module is an MxB crossbar switch (Fig 2b, element 20, input stage; elements 21 (for M inputs of input stage), 25 (for B outputs of

input stage); column 6, lines 54 – 61), and the output module is a BxN crossbar switch (Fig 2b, element 22, output stage; elements 27 (for B inputs of output stage), 23 (for N outputs of output stage); column 6, lines 54 – 61).

Regarding claims 5, 16, Yang et al. disclose the limitation of the packet switch as recited in claimed further including a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers (Fig. 4, column 11, lines 32 – 37).

Regarding claims 9, 20, Yang et al. discloses the limitation of the packet switch as recited in claimed wherein each of the B registers is a circular shift register (column 12, line 35).

5. Claims 3, 4, 6 – 8, 10 – 11, 14, 15, 17 – 19, 22 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (U.S. 5801641 B1) in view of Eng et al. (U.S.4955017) as applied to claims 1, 2, 5, 9, 12, 13, 16, 20, 21, 24, above, and further in view of Holden (U.S. Patent No. 5583861).

Regarding claims 3, 14, Yang et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (column 3, lines 52 – 57; column 6, lines 54 – 61), Yang et al. does not disclose expressly the packet switch as recited in claimed wherein the packet buffer is a one-stop shared buffer memory. Holden discloses the limitation of the packet switch as recited in claimed wherein the packet buffer is a one-stop shared buffer memory (Abstract, lines 4 – 6). It would have been obvious to modify Yang et al. to include the

packet switch as recited in claimed wherein the packet buffer is a one-stop shared buffer memory such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 4, 15, 22, Yang et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (column 3, lines 52 – 57; column 6, lines 54 – 61), Yang et al. does not disclose expressly the packet switch as recited in claimed further including queues and their identifiers to store the destination addresses and wherein the output module transfers N_1 packets from the occupied registers in each of the frame times to N_2 output ports indicated by identifiers of the queues, $N_1 \leq N_2 \leq N$. Holden discloses the limitation of the packet switch as recited in claimed further including queues and their identifiers to store the destination addresses (column 6, lines 45– 49; column 5, lines 38– 45; column 2, lines 20 – 26) and wherein the output module transfers N_1 packets from the occupied registers in each of the frame times to N_2 output ports indicated by identifiers of the queues, $N_1 \leq N_2 \leq N$ (column 7, lines 1 – 19; lines 27 – 35; lines 46 – 56). It would have been obvious to modify Yang et al. to include a packet switch as recited in claimed further including queues and their identifiers to store the destination addresses and wherein the output module transfers N_1 packets from the occupied registers in each of the frame times to N_2 output ports indicated by identifiers of the queues, $N_1 \leq N_2 \leq N$

such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 6, 17, Yang et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (column 3, lines 52 – 57; column 6, lines 54 – 61), Yang et al. does not disclose expressly the packet switch as recited in claimed further including M header hoppers, coupled to the input module, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times. Holden discloses the limitation of the packet switch as recited in claimed further including M header hoppers, coupled to the input module, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times (column 5, lines 38 – 46; lines 58 – 67). It would have been obvious to modify Yang et al. to include a packet switch as recited in claim 5 further including M header hoppers, coupled to the input module, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 7, 18, Yang et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N

output ports (column 3, lines 52 – 57; column 6, lines 54 – 61), Yang et al. does not disclose expressly the packet switch as recited in claimed further including N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information of the packets. Holden discloses the limitation of the packet switch as recited in claimed further including N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information of the packets (column 5, lines 38 – 51; column 6, lines 45 – 49). It would have been obvious to modify Yang et al. to include a packet switch as recited in claim 6 further including N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information of the packets such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 8, 11, 19, Yang et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (column 3, lines 52 – 57; column 6, lines 54 – 61), Yang et al. does not disclose expressly the packet switch as recited in claimed wherein the header hoppers, the register selector, and the queues are coupled via a multi-user bus. Holden discloses the limitation of the packet switch as recited in claimed wherein the header hoppers, the register selector, and the queues are coupled via a multi-user bus (Fig. 5,

element "Back pressure"; column 7, lines 33 – 35; column 9, lines 5 – 8). It would have been obvious to modify Yang et al. to include a packet switch as recited in claim 7 wherein the header hoppers, the register selector, and the queues are coupled via a multi-user bus such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claim 10, Yang et al. discloses the limitation of a MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports, the switch comprising a MxB input crossbar switch, B>M, for switching the M input packets to M of the B outputs to produce M switched packets during each of the frame times (column 3, lines 52 – 57; column 6, lines 54 – 61), a BxN output crossbar switch coupled to the packet buffer, for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses (Fig. 2B, element 22, output stage; column 11, lines 32 – 37). Yang et al. and Eng et al. do not disclose expressly a one-stop shared buffer memory, including B registers, coupled to the input crossbar switch, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets, a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers, M header hoppers, coupled to the input crossbar switch, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times, and N queues for storing the addresses of the assigned registers in

each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information. Holden discloses the limitation of a one-stop shared buffer memory (Abstract, lines 4 – 6), including B registers, coupled to the input crossbar switch, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets (column 6, lines 41 – 44), a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers (column 5, lines 58 – 62; column 15, lines 24 – 26), M header hoppers, coupled to the input crossbar switch (column 5, lines 39 – 44; lines 58 – 62), for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times (column 16, lines 32 – 40), and N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information (column 15, lines 24 – 39). It would have been obvious to modify Yang et al. and Eng et al. to include a one-stop shared buffer memory, including B registers, coupled to the input crossbar switch, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets, a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers, M header hoppers, coupled to the input crossbar switch, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times, and N queues for storing the addresses of the assigned registers in

each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claim 23, Yang et al. discloses the limitation of a method for switching M input packets arriving in each of a sequence of frame times to N output ports using an MXN packet switch (column 3, lines 52 – 57; column 6, lines 54 – 61), the method comprising prior to the arrival of the M input packets in each one of the frame times, selecting M available registers in a packet buffer having B registers, B > M, to store the M input packets arriving in the next one of the frame times (column 11, lines 15 – 37), setting up connections in an input module to switch the M input packets to the M available registers, delivering and storing the M input packets to the M available registers using the connections of the input module (column 11, lines 15 – 29). Yang et al. and Eng et al. do not disclose expressly transmitting the register addresses of the M available registers to header hoppers, sending headers from the M input packets to the header hoppers, transmitting the register addresses from the headers of the M input packets to N queues corresponding to destination addresses in the headers of the M input packets, updating the queues based on the header information provided by the header hoppers, sending control information to a register selector to inform the register selector of the destination addresses of the M input packets in each of the frame times, selecting up to N stored packets from the packet buffer for each of the destination addresses based on contents of the queues, transmitting the up to N selected stored

packets to the outputs, updating the register selector to account for any remaining destination addresses for each stored packet, and transmitting any remaining stored packets to the N outputs in subsequent one or more subsequent frames to clear the remaining stored packets. Holden discloses the limitation of transmitting the register addresses of the M available registers to header hoppers, sending headers from the M input packets to the header hoppers (Fig. 4, column 5, lines 29 – 38), transmitting the register addresses from the headers of the M input packets to N queues corresponding to destination addresses in the headers of the M input packets, updating the queues based on the header information provided by the header hoppers (Fig. 4, column 5, lines 38 – 46), sending control information to a register selector to inform the register selector of the destination addresses of the M input packets in each of the frame times, selecting up to N stored packets from the packet buffer for each of the destination addresses based on contents of the queues (column 5, lines 46 – 51; column 6, lines 32 – 43), transmitting the up to N selected stored packets to the outputs, updating the register selector to account for any remaining destination addresses for each stored packet, and transmitting any remaining stored packets to the N outputs in subsequent one or more subsequent frames to clear the remaining stored packets (column 7, lines 27 – 35, lines 46 – 56). It would have been obvious to modify Yang et al. and Eng et al. to include transmitting the register addresses of the M available registers to header hoppers, sending headers from the M input packets to the header hoppers, transmitting the register addresses from the headers of the M input packets to N queues corresponding to destination addresses in the headers of the M input packets, updating

the queues based on the header information provided by the header hoppers, sending control information to a register selector to inform the register selector of the destination addresses of the M input packets in each of the frame times, selecting up to N stored packets from the packet buffer for each of the destination addresses based on contents of the queues, transmitting the up to N selected stored packets to the outputs, updating the register selector to account for any remaining destination addresses for each stored packet, and transmitting any remaining stored packets to the N outputs in subsequent one or more subsequent frames to clear the remaining stored packets such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ACL

Oct 05, 2005

Ajit Patel
Primary Examiner